

Amendments to the Claims

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims

1-38. (Canceled)

39. (Currently Amended) A semiconductor device comprising:
a semiconductor substrate;
a channel region formed in said semiconductor substrate;
source and drain regions in said channel region semiconductor substrate wherein said channel region is located between said source and drain regions;
at least first and second pinning impurity regions formed in said semiconductor substrate wherein said first and second pinning impurity regions are formed in a vicinity of a boundary between said channel region and one of the source and drain regions[[,]] and is doped with an impurity of a conductivity type opposite to said source and drain regions; and wherein an energy band of each of the first and second pinning regions is shifted from that of other portions of the channel region;
a gate insulating film formed over the channel region; and
a gate electrode over the channel region with the gate insulating film interposed therebetween,
wherein said first and second pinning impurity regions are separated from each other, arranged along said boundary and are of a conductivity type which is opposite to said source and drain regions.

40. (Currently Amended) The semiconductor device according to claim 39 wherein said first and second pinning impurity regions contain [[an]] the impurity at a concentration within a range of 1×10^{17} to 5×10^{19} atoms/cm³.

41. (Currently Amended) The semiconductor device according to claim 39 wherein a width of said first and second pinning impurity regions along said boundary is 0.05 to 0.3 μm .

42. (Currently Amended) The semiconductor device according to claim 39 wherein an interval between said first and second pinning impurity regions is 0.04 to 0.6 μm .

43. (Currently Amended) A semiconductor device comprising:
a semiconductor substrate;
a channel region formed in said semiconductor substrate;
source and drain regions in said channel-region semiconductor substrate wherein said channel region is located between said source and drain regions;
at least first and second pinning impurity regions formed in said semiconductor substrate wherein said first and second pinning impurity regions are formed in a vicinity of a first boundary between said channel region and the source region and are separated from each other; and wherein an energy band of each of the first and second pinning regions is shifted from that of other portions of the channel region;
at least third and fourth pinning impurity regions formed in said semiconductor substrate wherein said third and fourth pinning impurity regions are formed in a vicinity of a second boundary between said channel region and the drain region and are separated from each other;
a gate insulating film formed over the channel region; and
a gate electrode over the channel region with the gate insulating film interposed therebetween,
wherein said first and second pinning regions are arranged along said first boundary and said third and fourth pinning regions are arranged along said second boundary, and a conductivity type each of said first, second, third and fourth pinning impurity regions is doped with an impurity [[are]] of a conductivity type opposite to that of said source and drain regions.

44. (Currently Amended) The semiconductor device according to claim 43 wherein said first and second pinning impurity regions contain an impurity at a concentration within a range of 1×10^{17} to 5×10^{19} atoms/cm³.

45. (Currently Amended) The semiconductor device according to claim 43 wherein said third and fourth pinning impurity regions contain an impurity at a concentration within a range of 1×10^{17} to 5×10^{19} atoms/cm³.

46. (Currently Amended) The semiconductor device according to claim 43 wherein a width of said first and second pinning impurity regions along said boundary is 0.05 to 0.3 μm .

47. (Currently Amended) The semiconductor device according to claim 43 wherein a width of said third and fourth pinning impurity regions along said boundary is 0.05 to 0.3 μm .

48. (Currently Amended) The semiconductor device according to claim 43 wherein an interval between said first and second pinning impurity regions is 0.04 to 0.6 μm .

49. (Currently Amended) The semiconductor device according to claim 43 wherein an interval between said third and fourth pinning impurity regions is 0.04 to 0.6 μm .

50. (Currently Amended) A semiconductor device comprising:
a semiconductor substrate;
a channel region formed in said semiconductor substrate;
source and drain regions in said channel region wherein said channel region is located between said source and drain regions;

at least first and second pinning impurity regions formed in said semiconductor substrate wherein said first and second pinning impurity regions are formed in a vicinity of a boundary between said channel region and one of the source and drain regions, and wherein an energy band of each of the first and second pinning regions is shifted from that of other portions of the channel region;

a gate insulating film formed over the channel region; and
a gate electrode over the channel region with the gate insulating film interposed
therebetween,

wherein said first and second pinning impurity regions are arranged along said boundary
separated from each other and are doped with an impurity [[are]] of a conductivity type which is
opposite to said source and drain regions, and

wherein said first and second pinning regions are overlapped by said gate electrode at
least partly.

51. (Currently Amended) The semiconductor device according to claim 50 wherein said
first and second pinning impurity regions contain an impurity at a concentration within a range
of 1×10^{17} to 5×10^{19} atoms/cm³.

52. (Currently Amended) The semiconductor device according to claim 50 wherein a
width of said first and second pinning impurity regions along said boundary is 0.05 to 0.3 μm .

53. (Currently Amended) The semiconductor device according to claim 50 wherein an
interval between said first and second pinning impurity regions is 0.04 to 0.6 μm .

54. (Currently Amended) A semiconductor device comprising:
a semiconductor substrate;
a channel region formed in said semiconductor substrate;
source and drain regions in said channel region semiconductor substrate wherein said
channel region is located between said source and drain regions wherein each of said source and
drain regions [[are]] provided with a metal silicide layer on a surface thereof,
at least first and second pinning impurity regions formed in said semiconductor substrate
wherein said first and second pinning impurity regions are formed in a vicinity of a boundary
between said channel region and one of the source and drain regions and are separated from each
other;, and wherein an energy band of each of the first and second pinning regions is shifted
from that of other portions of the channel region;

- a gate insulating film formed over the channel region; and
a gate electrode over the channel region with the gate insulating film interposed
therebetween,
wherein said first and second pinning regions are arranged along said boundary and are
doped with an impurity of a conductivity type which is opposite to said source and drain regions.
55. (Previously Presented) The semiconductor device according to claim 54 wherein said metal silicide layer comprises titanium silicide.
56. (Currently Amended) The semiconductor device according to claim 54 wherein said first and second pinning regions contain [[an]] the impurity at a concentration within a range of 1×10^{17} to 5×10^{19} atoms/cm³.
57. (Currently Amended) The semiconductor device according to claim 54 wherein a width of said first and second pinning impurity regions along said boundary is 0.05 to 0.3 μ m.
58. (Currently Amended) The semiconductor device according to claim 54 wherein an interval between said first and second pinning impurity regions is 0.04 to 0.6 μ m.
59. (Currently Amended) The semiconductor device according to claim 39 further comprising at least third and fourth pinning impurity regions formed in said semiconductor substrate wherein said third and fourth pinning impurity regions are formed in a vicinity of a second boundary between said channel region and the other one of the source and drain regions and said third and fourth pinning impurity regions are arranged along said second boundary separated from each other and are doped with an impurity of a conductivity type which is opposite to said source and drain regions.
60. (Currently Amended) The semiconductor device according to claim 50 further comprising at least third and fourth pinning impurity regions formed in said semiconductor substrate wherein said third and fourth pinning impurity regions are formed in a vicinity of a

second boundary between said channel region and the other one of the source and drain regions and said third and fourth pinning impurity regions are arranged along said second boundary separated from each other and are doped with an impurity of a conductivity type which is opposite to said source and drain regions.

61. (Currently Amended) The semiconductor device according to claim 54 further comprising at least third and fourth pinning impurity regions formed in said semiconductor substrate wherein said third and fourth pinning impurity regions are formed in a vicinity of a second boundary between said channel region and the other one of the source and drain regions and said third and fourth pinning regions are arranged along said second boundary separated from each other and are doped with an impurity of a conductivity type which is opposite to said source and drain regions.

62-65. (Canceled)